A

ASSISTANT COMMISSIONER FOR PATENTS   Docket No.: **061607-1100**
Washington, D.C. 20231

Sir: Transmitted herewith for filing is the patent application of

Inventors: **Louis F. Villarosa and Mark D. Studebaker**

For: **CIRCUIT AND METHOD FOR DETECTING AND CORRECTING DATA CLOCKING ERRORS**

Enclosed are the following documents:

13   Pages of Specification
4   Pages of Claims
1   Page of Abstract
8   Sheets of Drawings (Formal)
☒   An Assignment of the Invention To: Paradyne Corporation
☒   Recordation Cover Sheet
☒   Combined Declaration and Power of Attorney
☐   Petition to Make Special
☐   Declaration of Counsel
☐   Information Disclosure Statement and Form PTO-1449

CLAIMS AS FILED BY A LARGE ENTITY						
	Total Claims Presented		Claims Allowed in Basic Fee	Present Extra	Rate	Basic Fee: $760
Total Claims	15	Minus	20	0	x $ 18.00	$ 0.00
Indep. Claims	3	Minus	3	0	x $ 78.00	$ 0.00
☐ First Presentation of multiple Dependent Claims					+ $ 260.00	$
☐ Surcharge - Late Filing of Fee and/or Declaration					+ $ 130.00	$
☐ Assignment Recordation Fee					+ $ 40.00	$
					Total Filing Fee	$ 760.00

☒   Please Charge Paradyne Corporation's Deposit Account No. 16-0255 in the Amount of
$760.00. A Duplicate Copy is Enclosed.

☒   The Commissioner is Hereby Authorized to Charge any Additional Fees Which may Be Required to Paradyne
Corporation's Deposit Account No. 16-0255. The Commissioner is requested to credit any overpayment to
Paradyne Corporation's Deposit Account No. 16-0255. A duplicate Copy of this Sheet is Enclosed.
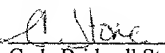
**THOMAS, KAYDEN, HORSTEMEYER
& RISLEY, L.L.P.**
100 Galleria Parkway, Suite 1500   Dan R. Gresham
Atlanta, Georgia 30339-5948   Registration No. 41,805
(770) 933-9500

5

10   TO ALL WHOM IT MAY CONCERN

Be it known that we, Louis F. Villarosa, Jr., residing at 2718 Palmetto St., Tampa,

Hillsborough County, Florida, and Mark D. Studebaker, 3042 Kevlyn Ct., Safety Harbor,

Pinellas County, Florida, citizens of the United States of America, have invented certain new

and useful improvements in a

15

CIRCUIT AND METHOD FOR DETECTING
AND CORRECTING DATA CLOCKING ERRORS

of which the following is a specification.

20

CIRCUIT AND METHOD FOR DETECTING
AND CORRECTING DATA CLOCKING ERRORS

CROSS REFERENCE TO RELATED APPLICATIONS

5   This application claims priority to and the benefit of the filing date of co-pending and commonly assigned provisional application entitled CIRCUIT FOR AUTOMATICALLY INVERTING DATA CLOCK SIGNAL UPON DETECTION OF DATA CLOCKING ERROR, assigned serial number 60/101,467, filed September 23, 1998, which is hereby incorporated by reference.

10

TECHNICAL FIELD

The present invention relates generally to communication networks, and more particularly, to a data communication system having the capability of detecting and dynamically correcting clocking errors attributable to system delays.

15

BACKGROUND OF THE INVENTION

In the field of data communications, data terminal equipment (DTE) is the source or destination of data in a communication connection. The DTE is typically connected to data communication equipment (DCE), which is in turn connected to the communication channel.

20   The DTE may be a dumb terminal or printer, however in most modern communication networks, the DTE is typically a computer, a bridge, or a router, which interconnects local area networks (LANs).

DCEs are typically modems or other types of communication devices. The DCE resides between the DTE and a communication channel. The DCE provides a connection for

25   the DTE to send and receive data to and from the communication channel. Additionally, the DCE provides clocking to the DTE. In an analog communication network, such as a plain old telephone service (POTS) network, the DCE is typically a modem. In a digital

1

communication network, such as a frame relay network, the DCE is typically a CSU/DSU (channel service unit/data service unit).

DTE and DCE interfaces are defined by the physical layer in the OSI (Open Systems Interconnection) model. The most common standards for DTE/DCE devices are EIA 5 (Electronic Industries Association) RS-232-C and RS-232-D. Outside the United States, these standards are the same as the V.24 standard of the CCITT. Other DTE/DCE standards include the EIA RS-366-A, as well as the CCITT X.20, X.21, and V.35 standards. The later standards are used for high-speed communication over telephone lines.

As noted, clocking is provided by the DCE to the DTE. The DCE sends a clocking 10 signal to the DTE, and the DTE responds by sending data synchronously with the clocking signal. Theoretically, there is perfect timing between the clocking signal transmitted by the DCE and the synchronous data signal transmitted by the DTE. In practice, however, there is some delay before the DTE data signal is transmitted. This delay is attributable to such factors as the physical proximity of the DCE and the DTE, the length of the cable connecting 15 the DCE and the DTE, and temperature changes in the system.

Fig. 1 is a schematic view illustrating a typical prior art communication environment 5 in which a DTE 12 is interfaced to a communication channel 11 by a DCE 13. In the communication environment 5 illustrated in Fig. 1, the DCE 13 employs a typical prior art clocking circuit. A clock source 18 generates a timing signal (DCE ST), which is sent from 20 the DCE 13 to the DTE 12 on connection 15. In response to signal DCE ST, the DTE 12 sends a data signal (DTE SD) to the DCE 13 on connection 16. The DCE 13 samples signal DTE SD in data latch 17. A clocking signal (SD LATCH CLK) is also provided by clock source 18 to data latch 17 on connection 14. The SD LATCH CLK signal is used to clock the sampling of signal DTE SD in data latch 17.

25 As illustrated in Fig. 1, in prior art systems the same clocking signal is typically used for signal DCE ST and signal SD LATCH CLK. However, in most installations connections

2

15 and 16 typically are much longer than connection 14. Thus, signals DCE ST and DTE SD typically are required to traverse much greater physical distances than signal SD LATCH CLK. As a result, signal DTE SD may be delayed in reaching data latch 17 relative to signal SD LATCH CLK. Temperature changes in the system may also result in varying delays.

5   Because data is sampled by the DCE 13 at clock transitions, if delays in the system become significant compared to the frequency of the data signal, data clocking errors may occur as follows: the DCE 13 may double sample the data, or the DCE 13 may miss sampling the data altogether. Such errors are more likely to occur as the data rate increases. This is especially troublesome as network designers strive for higher and higher data rates.

10   Fig. 2 is a graphical illustration of the DCE ST, DTE SD, and SD LATCH CLK signals of the communication environment 5 of Fig. 1. Signal DTE SD is sampled in data latch 17 (of Fig. 1) on the rising edge of the SD LATCH CLK signal. System delays, such as those discussed above, can cause data latch 17 to sample signal DTE SD at a transition in signal DTE SD. The sampling point for this condition is illustrated in Fig. 2 by reference

15   numeral 19.

       With reference back to Fig. 1, the effects of the above-described delay may be alleviated in some instances by sending signal SD LATCH CLK from the DCE 13 to the DTE 12 and having DTE 12 return signal SD LATCH CLK back to DCE 13. The DCE 13 then uses the returned clock signal (rather than the original clock signal) to sample the data. In this

20   way, the time delay between the clock signal used for sampling and the DTE data signal is minimized. This type of timing scheme is typically referred to as terminal timing.

       When the DTE does not have terminal timing capability, another way of addressing delay errors is by manually inverting the phase of the DCE's internal clock (*i.e.*, signal SD LATCH CLK on connection 14 of Fig. 1) relative to the clock provided to the DTE (*i.e.*,

25   signal DCE ST on connection 15 of Fig. 1), so that signal DTE SD is sampled in the middle of the DCE's internal clock cycle rather than at a transition point. However, the efficacy of this

method depends on the amount of delay in the system, which may differ depending on the specific installation. Each site must be evaluated and the manual inversion must be done on a site by site basis during installation, depending on the configuration of each site. However, post-installation changes in the DTE cable, in the DTE itself, or elsewhere in the system, can

5 cause changes in the amount of delay present in the system. In such cases, subsequent manual intervention is required to adjust the clock phase.

Thus, there is a need in the industry for a circuit and method that detect clocking errors between DCEs and DTEs, and dynamically adjust the clock phase to eliminate such errors.

10 **SUMMARY OF THE INVENTION**

A circuit and method are presented that permit a DCE connected to a DTE to detect the condition in which the data signal transmitted to the DCE from the DTE is sampled near the transition of the data signal. Upon detecting this condition, the DCE's clocking signal is inverted relative to the DTE's data signal to ensure that that the DTE's data signal is sampled

15 near the midpoint between data signal transitions. This is accomplished by obtaining two samples of the DTE's data signal during a time interval that is less than the period of the DCE's clocking signal. The time interval between the two samples is typically on the order of 1/8 of the period of the DCE's clocking signal. The two samples are then compared with each other. If the two samples are different, it is apparent that there was a transition in the

20 DTE data signal during the time interval, which indicates a clocking error. If a clocking error is indicated, the invention automatically corrects the error by inverting the DCE's clocking signal relative to the DTE's data signal so that the sampling point is moved away from the transition of the DTE's data signal.

An advantage of the invention is that it automatically eliminates clocking errors in

25 systems in which the DTE does not have terminal timing capability.

Another advantage of the invention is that it is automatic and requires no manual intervention.

Another advantage of the invention is that it dynamically adjusts to changes in a system, such as cabling changes and temperature changes.

5   Other features of the present invention will become apparent to one with skill in the art upon examination of the following drawings and detailed description. It is intended that all such additional features be included herein within the scope of the present invention.

BRIEF DESCRIPTION OF THE SEVERAL
10   ## VIEWS OF THE DRAWINGS

The invention can be better understood with reference to the following drawings. The components in the drawings are not necessarily to scale, emphasis instead being placed upon clearly illustrating the principles of the present invention. Moreover, in the drawings, like
15   reference numerals designate corresponding parts throughout the several views.

Fig. 1 is a schematic view illustrating a typical communication environment in which a DCE employing a typical prior art clocking circuit is used to interface a DTE to a communication channel;

Fig. 2 is a graphical illustration of the data and clock signals of the clocking circuit of
20   Fig. 1;

Fig. 3 is a schematic view illustrating a typical communication environment in which a DCE employing the clocking circuit of the present invention is used to interface a DTE to a communication channel;

Fig. 4 is a schematic view illustrating a first embodiment of the clocking circuit of Fig.
25   3;

Fig. 5 is a schematic view illustrating a second embodiment of the clocking circuit of Fig. 3;

Fig. 6 is a graphical illustration of the data and clock signals of the clocking circuits of Figs. 3, 4 and 5;

Fig. 7 is a graphical illustration of the sampling period of a first embodiment of the clocking circuits of Figs. 4 and 5; and

5   Fig. 8 is a graphical illustration of the sampling period of a second embodiment of the clocking circuits of Figs. 4 and 5.

DETAILED DESCRIPTION OF THE INVENTION

Reference will now be made in detail to the description of the invention as illustrated
10   in the drawings. While the invention will be described in connection with these drawings, there is no intent to limit it to the embodiment or embodiments disclosed therein. On the contrary, the intent is to cover all alternatives, modifications and equivalents included within the spirit and scope of the invention as defined by the appended claims.

Fig. 3 is a schematic view illustrating a typical communication environment 10 in
15   which a DCE 23 employing the clocking circuit 20 of the present invention is used to interface a DTE 22 to a communication channel 21. Clocking circuit 20 generates a timing signal DCE ST, which is sent from the DCE 23 to the DTE 22 on connection 25. In response to signal DCE ST, the DTE 22 sends data signal DTE SD to the DCE 23 on connection 26. The clocking circuit 20 samples signal DTE SD and generates a reclocked signal corresponding to
20   signal DTE SD (*i.e.*, signal RCLK DTE SD), which is provided to data latch 27 on connection 29. The DCE 23 samples signal RCLK DTE SD in data latch 27. Clocking signal SD LATCH CLK is also provided to data latch 27 by clocking circuit 20 on connection 24. The SD LATCH CLK signal is used to clock the sampling of signal RCLK DTE SD in data latch 27.

As will be discussed below with reference to Figs. 4 and 5, clocking circuit 20 detects
25   whether signal DTE SD is being sampled at a transition point, which can lead to data sampling errors. If such is the case, the circuit inverts either signal DCE ST or signal SD

LATCH CLK (but not both) so that the two signals are 180 degrees out of phase with respect to each other. By inverting one of these signals, the clocking circuit 20 ensures that signal DTE SD is not sampled at a transition point. By ensuring that signal DTE SD is not sampled at a transition point, the clocking circuit 20 automatically eliminates the data sampling errors

5   that may occur when a signal is sampled near its transition point.

Fig. 4 is a schematic view illustrating a first embodiment of the clocking circuit 20 of Fig. 3. In this embodiment, a master clock 31 generates a master clock signal, which is provided to clock generator 32 and to sample enable generator 34 on connection 33. The master clock 31 runs at a higher frequency than the clock generator 32. In a preferred

10   embodiment, the frequency of the master clock 31 is at least 8X the frequency of the clock generator 32. Clock generator 32 generates timing signals at a frequency equivalent to clock source 18 of Fig. 1. The output of clock generator 32 is signal DCE ST, which is provided to the DTE 22 (of Fig. 3) on connection 25.

Within clocking circuit 20, signal DCE ST is provided to one input of selector 40, as

15   well as to inverter 41, on connection 39. The output of inverter 41 (*i.e.*, an inverted version of signal DCE ST), is provided to another input of selector 40 on connection 42. Selector 40 is therefore able to select either signal DCE ST or an inverted version of signal DCE ST, as discussed hereinafter. The output signal of selector 40 (*i.e.*, the signal selected by selector 40), is a clocking signal (INT CLK) that is internal to the clocking circuit 20. The INT CLK

20   signal is provided on connection 43 to the following elements of clocking circuit 20: inverter 44, sample enable generator 34, and data latch 45.

The INT CLK signal is inverted by inverter 44. The output of inverter 44 is signal SD LATCH CLK, which is provided to data latch 27 of Fig. 3 on connection 24.

The clocking circuit 20 determines the phase of signal INT CLK relative to the phase

25   of signal DCE ST as follows: the master clock signal is provided to one input of sample enable generator 34 on connection 33. Signal INT CLK is provided to a second input of

sample enable generator 34 on connection 43. The sample enable generator 34 generates two output signals: signal S1 ENABLE is generated on connection 35, and signal S2 ENABLE is generated on connection 36. In one embodiment, signal S1 ENABLE is asserted on the rising edge of the INT CLK signal, and signal S2 ENABLE is asserted a defined number of master

5   clock periods later. In one embodiment of the invention, signal S2 ENABLE is asserted on the master clock period following assertion of signal S1 ENABLE. For a master clock 31 running at 8X the frequency of clock generator 32, this means that the time interval between the assertion of the S1 ENABLE signal and the assertion of the S2 ENABLE signal is 1/8 of the period of the SD LATCH CLK signal. The timing of this embodiment is illustrated in Fig.

10   7.

In an alternate embodiment of the invention, the S1 ENABLE signal is asserted one master clock period before the rising edge of the INT CLK signal. In this embodiment, the S2 ENABLE signal is asserted one master clock period after the rising edge of the INT CLK signal. The timing of this embodiment is illustrated in Fig. 8.

15   The S1 ENABLE signal is provided to a first input of sample comparator 37 on connection 35. The S2 ENABLE signal is provided to a second input of sample comparator 37 on connection 36. The DTE SD signal is provided to a third input of sample comparator 37 on connection 26. Sample comparator 37 compares the state of the DTE SD signal at the time that the S1 ENABLE signal is asserted with the state of the DTE SD signal at the time

20   that the S2 ENABLE signal is asserted. The time interval between the assertion of the S1 ENABLE signal and the assertion of the S2 ENABLE signal determines the window in which non-equal samples of the DTE SD signal constitute a data transition condition, thereby indicating a clocking error in the system.

Clocking circuit 20 also contains data latch 45. Data latch 45 uses the INT CLK signal

25   provided on connection 43 to latch the DTE SD signal provided on connection 26. As explained below, selector 40 selects either the DCE ST signal on connection 39 or the

inverted DCE ST signal on connection 42 as the INT CLK signal. This choice ensures that the rising edge of the INT CLK signal occurs at approximately the midpoint of the transitions of the DTE SD signal. Data latch 45 therefore latches the DTE SD signal without error. The output of data latch 45 is the RCLK DTE SD signal, which is provided to data latch 27 of Fig.

5   3 on connection 29.

Because transitions of signal RCLK DTE SD are coincident with the rising edge of the INT CLK signal, the INT CLK signal on connection 43 is inverted by inverter 44 to generate the SD LATCH CLK signal. Due to this inversion, the SD LATCH CLK signal has a rising edge at approximately the midpoint of the RCLK DTE SD signal. The SD LATCH CLK

10   signal is provided to data latch 27 of Fig. 3 on connection 24.

If the DTE SD signal does not undergo a transition during the interval between the assertion of the S1 ENABLE signal and the assertion of the S2 ENABLE signal, no clocking error is indicated. In this case, there is no need to change the phase of the DCE ST signal and the SD LATCH CLK signal relative to each other. Thus, the output of sample comparator 37,

15   which is connected to selector 40 on connection 38, remains unchanged and selector 40 continues to maintain the current phase of the INT CLK signal on connection 43 relative to the DCE ST signal on connection 25.

On the other hand, if the DTE SD signal undergoes a transition during the interval between the assertion of the S1 ENABLE signal and the assertion of the S2 ENABLE signal, a

20   clocking error is indicated. In this case, the output of sample comparator 37 changes, thereby directing the selector 40 to change the current phase of the INT CLK signal on connection 43 by 180 degrees. This causes data latch 45 to sample the DTE SD signal in the midpoint of the signal, rather than at a transition point (*i.e.*, the transition of the DTE SD signal now occurs ½ bit period away from the sampling point, which is clocked by the INT CLK signal). Because

25   the DTE SD signal is no longer sampled at a transition point, the clocking error is eliminated.

Fig. 5 is a schematic view illustrating a second embodiment of the clocking circuit 20 of Fig. 3. In this embodiment, a master clock 31 is used to generate a master clock signal on connection 33. The master clock signal drives clock generator 32. The master clock 31 runs at a higher frequency than clock generator 32. In a preferred embodiment, the frequency of

5   the master clock 31 is at least 8X the frequency of the clock generator 32. Clock generator 32 generates timing signals at a frequency equivalent to clock source 18 of Fig. 1. The output of clock generator 32 is the INT CLK signal. The INT CLK signal is provided on connection 39 to inverter 44. The INT CLK signal is inverted by inverter 44, thereby becoming the SD LATCH CLK signal, which is provided to data latch 27 of Fig. 3 on connection 24.

10   Within clocking circuit 20, the INT CLK signal is also provided to one input of selector 40, and to inverter 41, on connection 39. The output of inverter 41 (*i.e.*, an inverted version of the INT CLK signal), is provided to another input of selector 40 on connection 42. Selector 40 is therefore able to select either the INT CLK signal or the inverted version of the INT CLK signal as the DCE ST signal. The DCE ST signal is provided to DTE 22 of Fig. 3

15   on connection 25.

The clocking circuit 20 determines the phase of the INT CLK signal relative to the phase of the DCE ST signal as follows: the master clock signal is provided on connection 33 to one input of sample enable generator 34. The INT CLK signal is provided on connection 39 to a second input of sample enable generator 34. The sample enable generator 34 generates

20   two output signals: S1 ENABLE, on connection 35, and S2 ENABLE, on connection 36. In one embodiment of the invention, the S1 ENABLE signal is asserted on the rising edge of the INT CLK signal, and the S2 ENABLE signal is asserted a defined number of master clock periods later. In a preferred embodiment of the invention, the S2 ENABLE signal is asserted on the master clock period following the assertion of the S1 ENABLE signal. For a master

25   clock 31 running at 8X the frequency of clock generator 32, the time interval between the

assertion of the S1 ENABLE signal and the assertion of the S2 ENABLE signal is 1/8 of the

SD LATCH CLK period. The timing for this embodiment is illustrated in Fig. 7.

In an alternative embodiment of the invention, the S1 ENABLE signal is asserted one

master clock period before the rising edge of the INT CLK signal. In this embodiment, the S2

5   ENABLE signal is asserted one master clock period after the rising edge of the INT CLK

signal. The timing for this embodiment is illustrated in Fig. 8.

The S1 ENABLE signal is provided on connection 35 to one input of sample

comparator 37. The S2 ENABLE signal is provided on connection 36 to a second input of

sample comparator 37. The DTE SD signal is provided on connection 26 to a third input of

10   sample comparator 37. Sample comparator 37 compares the state of the DTE SD signal at the

time that the S1 ENABLE signal is asserted with the state of the DTE SD signal at the time

that the S2 ENABLE signal is asserted. The time interval between the assertion of the S1

ENABLE signal and the assertion of the S2 ENABLE signal determines the window in which

non-equal samples constitute a data transition condition.

15   If the DTE SD signal does not undergo a transition during the interval between the

assertion of the S1 ENABLE signal and the assertion of the S2 ENABLE signal, no clocking

error is indicated. In this case, there is no need to change the phase of the DCE ST signal and

the INT CLK signal relative to each other. Therefore, the output of sample comparator 37,

which is connected to selector 40 on connection 38, remains the same and directs the selector

20   40 to maintain the current phase of the DCE ST signal relative to the INT CLK signal on

connection 39. The DCE ST signal is connected to the DTE 22 of Fig. 3 on connection 25.

On the other hand, if the DTE SD signal undergoes a transition during the interval

between the assertion of the S1 ENABLE signal and the assertion of the S2 ENABLE signal, a

clocking error is indicated. In this case, the output of sample comparator 37 changes, thereby

25   directing the selector 40 to change by 180 degrees the current phase of the DCE ST signal

provided to the DTE 22 of Fig. 3 on connection 25. Due to the phase shift in the DCE ST

signal, timing of the DTE SD signal on connection 26 is altered so that the DTE SD signal no longer undergoes a transition during the time interval between assertion of the S1 ENABLE signal and the assertion of the S2 enable signal.

The INT CLK signal is also provided on connection 39 to data latch 45. Data latch 45 uses the INT CLK signal to latch the DTE SD signal, which is provided to data latch 45 on connection 26. Because the DTE SD signal is sampled in data latch 45 on the rising edge of the INT CLK signal (which in this condition is the inverted version of the DCE ST signal), data latch 45 samples the DTE SD signal in the midpoint of the signal, rather than at a transition point (*i.e.*, the transition of the DTE SD signal, which is clocked by the INT CLK signal in data latch 45, now occurs ½ bit period away from the sampling point). Therefore data latch 45 latches the DTE SD signal without error. The output of data latch 45 is the RCLK DTE SD signal, which is provided to data latch 27 of Fig. 3 on connection 29.

Because transitions of the RCLK DTE SD signal are coincident with the rising edge of the INT CLK signal, the INT CLK signal must be inverted by inverter 44 to generate the SD LATCH CLK signal, which has a rising edge at the midpoint of the RCKL DTE SD signal. The SD LATCH CLK signal is provided to data latch 27 of Fig. 3 on connection 24.

Fig. 6 is a graphical illustration of the data and clock signals of the clocking circuit of Figs. 3, 4 and 5 when the DCE ST signal on connection 25 and the INT CLK signal (on connection 43 in Fig. 4 and on connection 39 in Fig. 5) are inverted relative to each other. As shown in Fig. 6, this inversion ensures that the DTE SD signal on connection 26 is sampled by latch 45 (as clocked by the INT CLK signal) away from a transition point of the DTE SD signal. This sampling point is indicated in Fig. 6 by reference numeral 51. The output of data latch 45, which is the RCLK DTE SD signal on connection 29, is then sampled in data latch 27 (as clocked by the SD LATCH CLK signal provided on connection 24), with the rising edge of the SD LATCH CLK signal occurring at the midpoint of the RCLK DTE SD signal

12

rather than at a transition of the RCLK DTE SD signal. This sampling point is indicated in Fig. 6 by reference numeral 52.

Fig. 7 is a graphical illustration of a first embodiment of the SD LATCH CLK signal and the timing of the S1 ENABLE and S2 ENABLE signals. In this embodiment, the rising

5   edge of the S1 ENABLE signal is coincident with the rising edge of the SD LATCH CLOCK signal, and the rising edge of the S2 ENABLE signal occurs at least 1/8 of the SD LATCH CLK period later.

Fig. 8 is a graphical illustration of a second embodiment of the SD LATCH CLK signal and the timing of the S1 ENABLE and S2 ENABLE signals for a master clock signal

10   that is 8X the frequency of the SD LATCH CLK signal. In this embodiment, the rising edge of the S1 ENABLE signal occurs 1/8 of the SD LATCH CLK period before the rising edge of the SD LATCH CLK signal, and the rising edge of the S2 ENABLE signal occurs 1/8 of the SD LATCH CLK period after the rising edge of the SD LATCH CLK signal. Thus, in this embodiment, the sampling interval between the assertion of the S1 ENABLE signal and the

15   assertion of the S2 ENABLE signal is ¼ of the period of the SD LATCH CLK.

It should be emphasized that the above-described embodiments of the present invention, particularly any "preferred" embodiments, are merely possible examples of implementations, merely set forth for a clear understanding of the principles of the invention. Many variations and modifications may be made to the above-described embodiment(s) of the

20   invention without departing substantially from the spirit and principles of the invention. For example, the master clock signal can be operated at frequencies other than 8X the frequency of the SD LATCH CLK signal, which will vary the sampling periods described above and illustrated in the Figures. All such modifications and variations are intended to be included herein within the scope of the present invention.

CLAIMS

Therefore, having thus described the invention, at least the following is claimed:

1. A circuit for detecting errors in the synchronization of a DTE (data terminal equipment) data signal with a DCE (data communication equipment) clocking signal, in a communication environment wherein the DCE interfaces the DTE to a communication channel at an interface rate determined by the DCE clocking signal, the circuit comprising:

a master clock producing a master clock signal having a frequency greater than the frequency of the DCE clocking signal;

a clock generator deriving a circuit clocking signal from said master clock signal, said circuit clocking signal having the same frequency as the DCE clocking signal;

a sample enable generator for generating a first sample enable signal at a first time and a second sample enable signal at a second time; and

a sample comparator for using said first sample enable signal and said second enable signal to obtain a first sample of said DTE data signal at said first time and a second sample of said DTE data signal at said second time, and for determining whether the DTE data signal has undergone a transition during the time interval between said first time and said second time.

2. The circuit of claim 1, wherein the frequency of said master clocking signal is approximately 8 times the frequency of said DCE clocking signal.

3. The circuit of claim 1, wherein the time interval between said first time and said second time is approximately 1/8 of the period of said DCE clocking signal.

1   4.   The circuit of claim 1, wherein said sample comparator generates a selector

2 control signal if said first sample is different from said second sample.

1   5.   The circuit of claim 4, further comprising:

2   an inverter producing an inverted circuit clocking signal from said circuit

3 clocking signal; and

4   a selector producing an output signal that is selected from the group consisting

5 of said circuit clocking signal and said inverted circuit clocking signal, in response to

6 said selector control signal.

1   6.   A circuit for detecting errors in the synchronization of a DTE (data terminal

2 equipment) data signal with a DCE (data communication equipment) clocking signal, in a

3 communication environment wherein the DCE interfaces the DTE to a communication

4 channel, the circuit comprising:

5   means for obtaining a first sample of said DTE data signal at a first time;

6   means for obtaining a second sample of said DTE data signal at a second time,

7 said second time being subsequent to said first time, the interval between said first

8 time and said second time being less than the period of the DCE clocking signal; and

9   means for comparing said first sample to said second sample.

1   7.   The circuit of claim 6, wherein the interval between said first time and said

2 second time is approximately 1/8 of the period of the DCE clocking signal.

1   8.   The circuit of claim 6, further comprising:

2   means for generating a selector control signal if said first sample is different

3 from said second sample.

15

1 9. The circuit of claim 8, further comprising:

2 means for inverting said DCE clocking signal in response to said selector

3 control signal.

1 10. The circuit of claim 9, further comprising:

2 means for transmitting said inverted DCE clocking signal from said DCE to

3 said DTE in lieu of said DCE clocking signal.

1 11. A method for detecting errors in the synchronization of a DTE (data terminal

2 equipment) data signal with a DCE (data communication equipment) clocking signal, in a

3 communication environment wherein the DCE interfaces the DTE to a communication

4 channel, the method comprising the steps of:

5 obtaining a first sample of said DTE data signal at a first time;

6 obtaining a second sample of said DTE data signal at a second time, said

7 second time being subsequent to said first time, the interval between said first time and

8 said second time being less than the period of the DCE clocking signal; and

9 comparing said first sample to said second sample.

1 12. The method of claim 11, wherein the interval between said first time and said

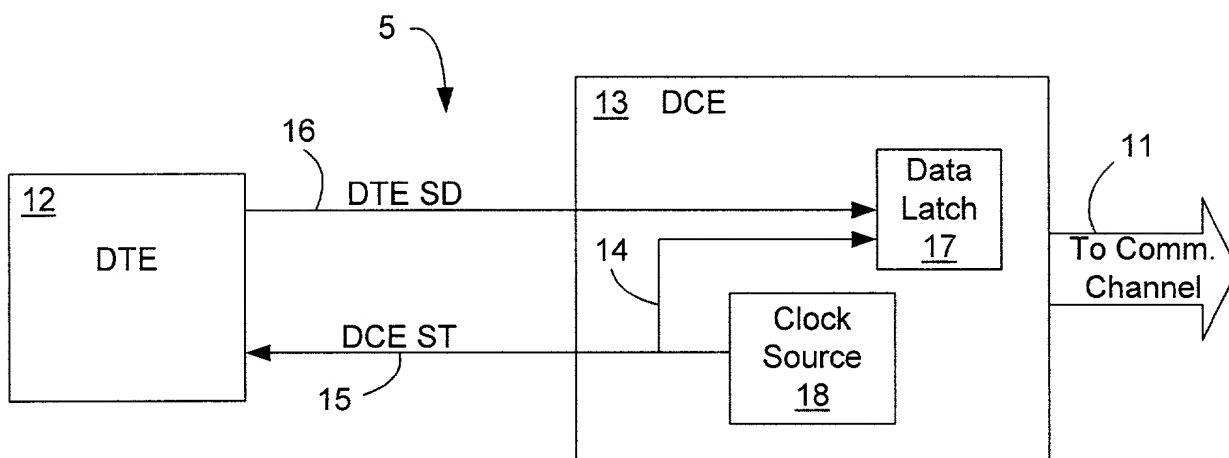2 second time is approximately 1/8 of the period of the DCE clocking signal.

1 13. The method of claim 11, further comprising the step of:

2 generating a selector control signal if said first sample is different from said
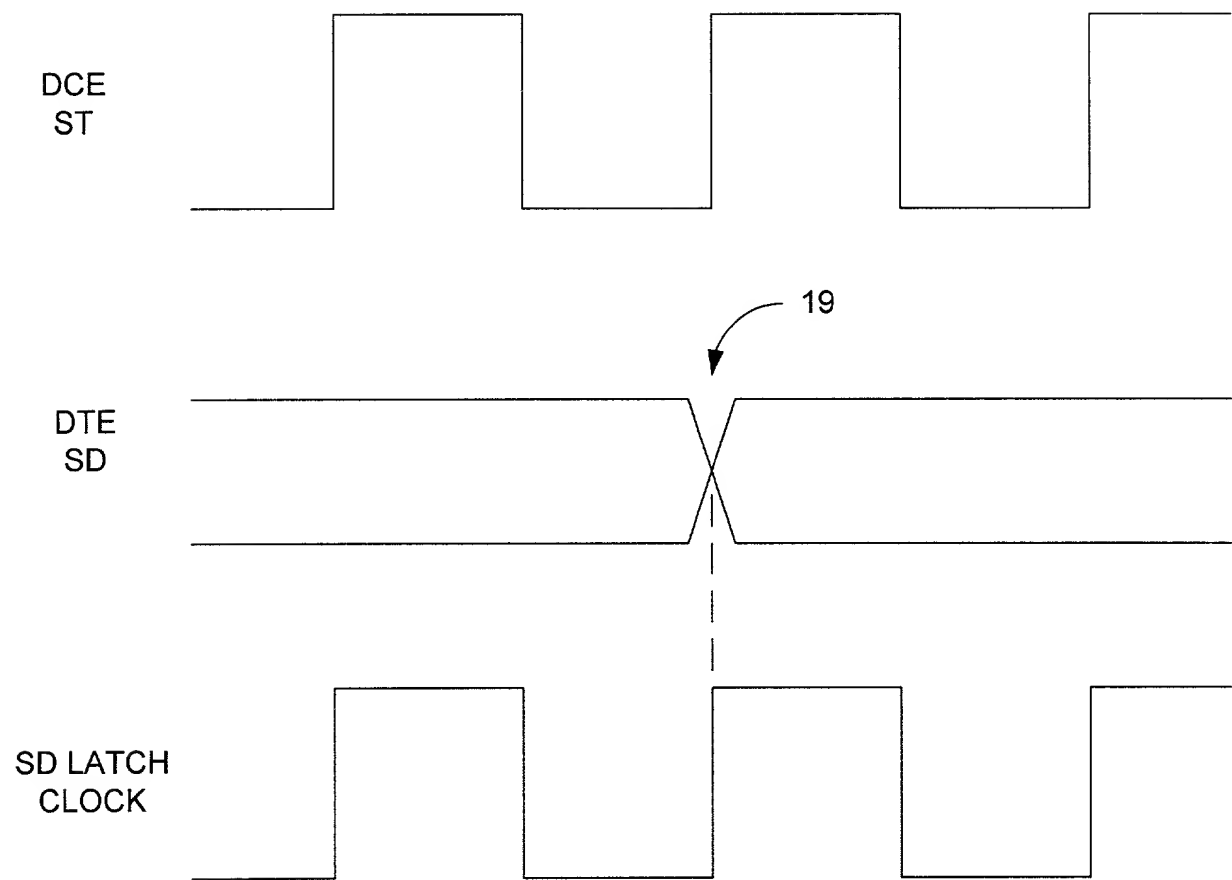
3 second sample.

1   14.   The method of claim 13, further comprising the step of:

2   inverting said DCE clocking signal in response to said selector control signal.

1   15.   The method of claim 14, further comprising the step of:

2   transmitting said inverted DCE clocking signal from said DCE to said DTE in

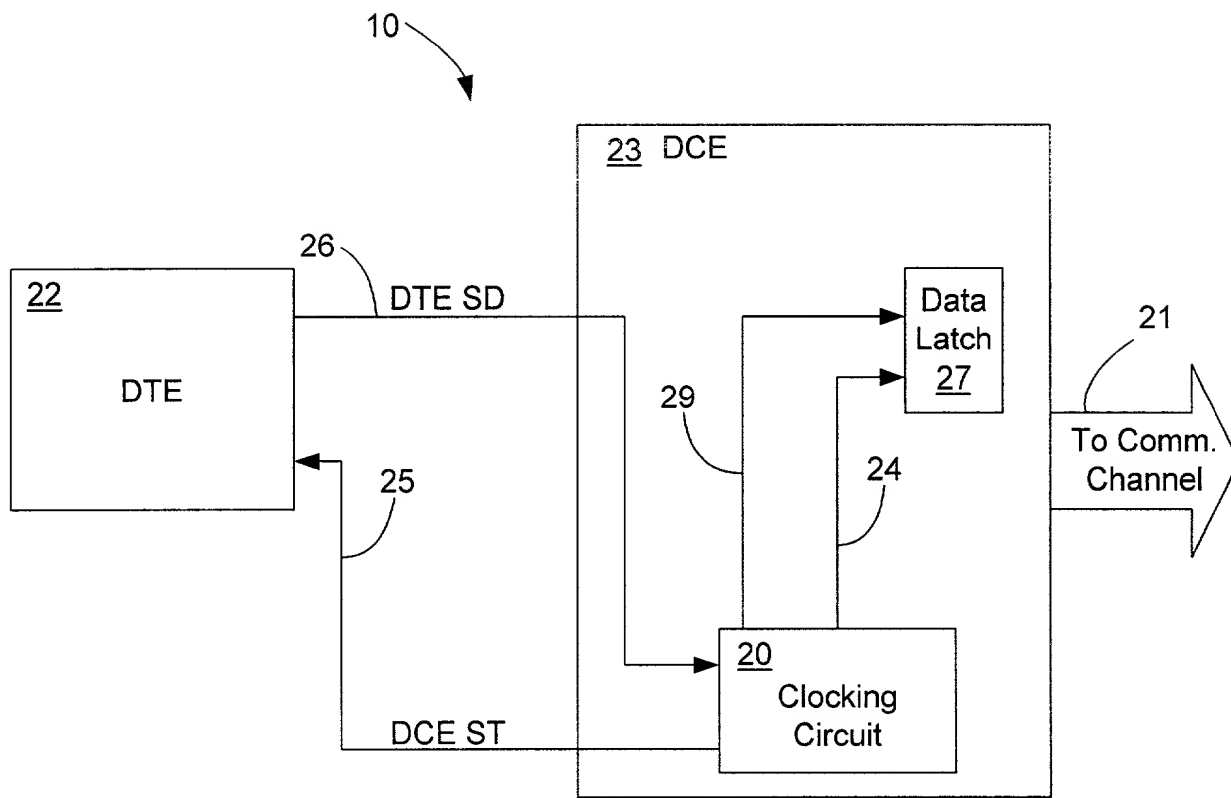3 lieu of said DCE clocking signal.

ABSTRACT OF THE DISCLOSURE

In a communications environment wherein data terminal equipment (DTE) transmits a data signal to data communication equipment (DCE) synchronously with a clocking signal provided by the DCE to the DTE, a circuit and method are configured to automatically detect a condition in which the data signal is sampled near a transition in the data signal, which may result in system clocking errors. Upon detecting this condition, the clocking signal used to sample the data signal is automatically inverted relative to the data signal to ensure that that the data signal is sampled near the midpoint between transitions in the data signal. In this manner, data clocking errors may be significantly reduced.
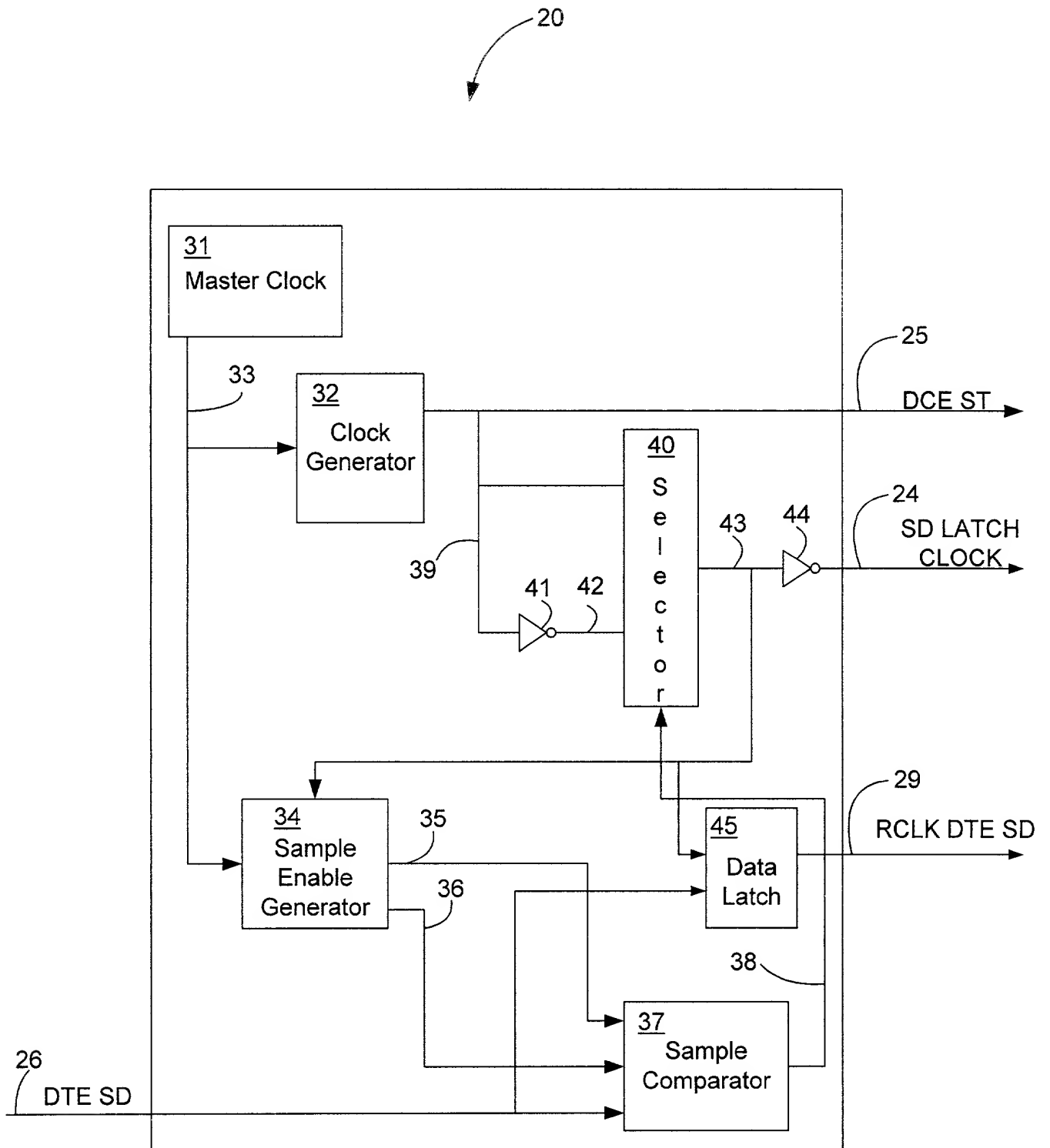
Fig. 1
(Prior Art)

DCE
ST

DTE
SD

19

SD LATCH
CLOCK

Fig. 2
(Prior Art)

10

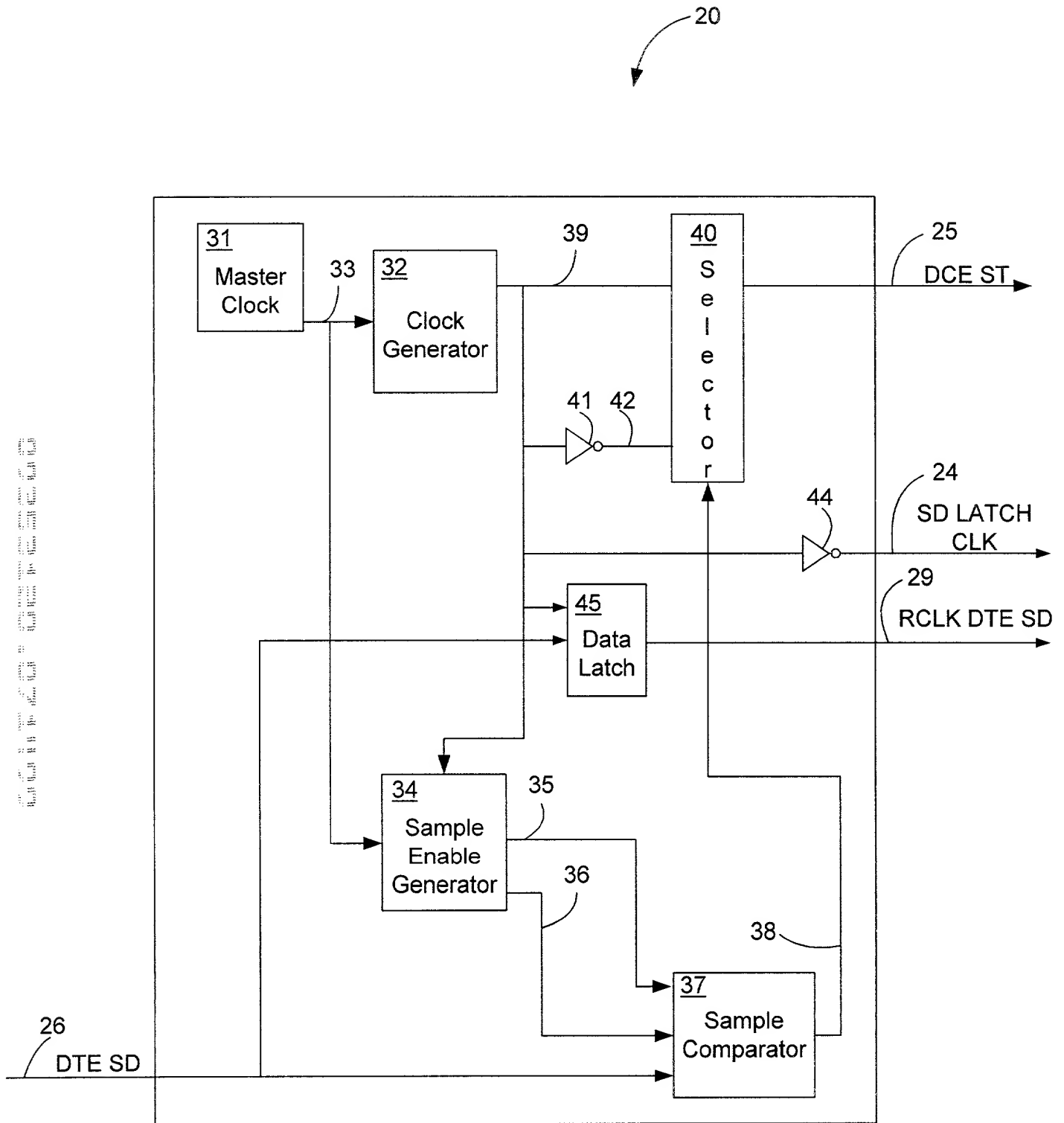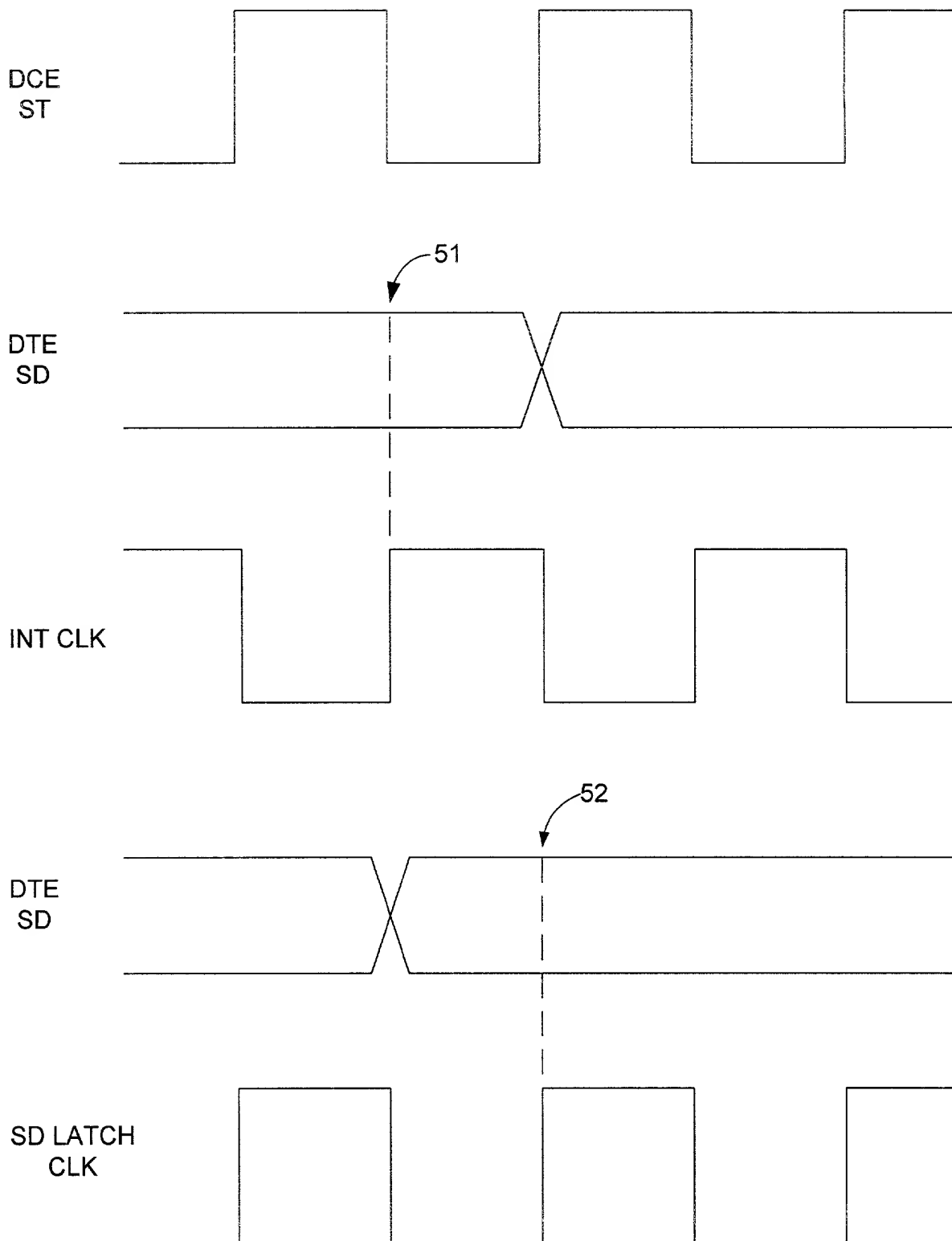23 DCE

26

22

DTE

DTE SD

25

Data
Latch
27

29

21

To Comm.
Channel

24

20

Clocking
Circuit

DCE ST

Fig. 3

Fig. 4

Fig. 5

DCE
ST

DTE
SD

51

INT CLK

DTE
SD

52

SD LATCH
CLK

Fig. 6

SD LATCH
CLOCK

≤ 1/8 SD LATCH CLOCK
PERIOD

S1 ENABLE   S2 ENABLE

Fig. 7

SD LATCH
CLOCK

≤ 1/4 SD LATCH CLOCK
PERIOD

S1 ENABLE   S2 ENABLE
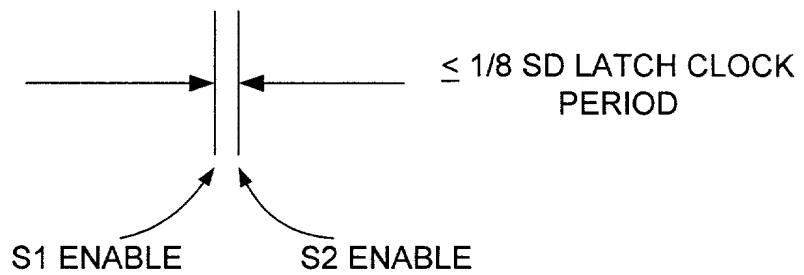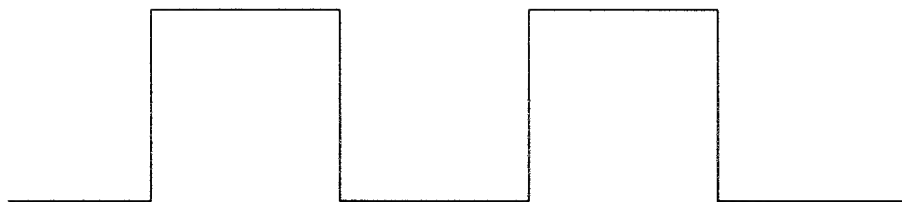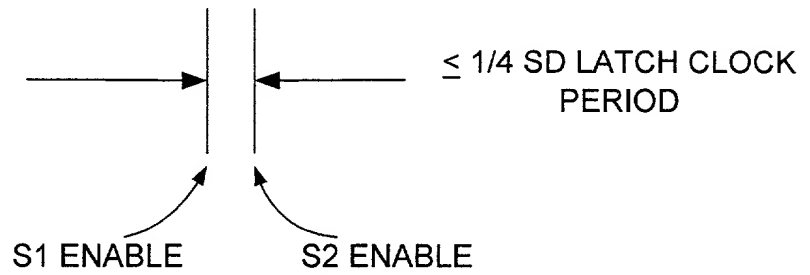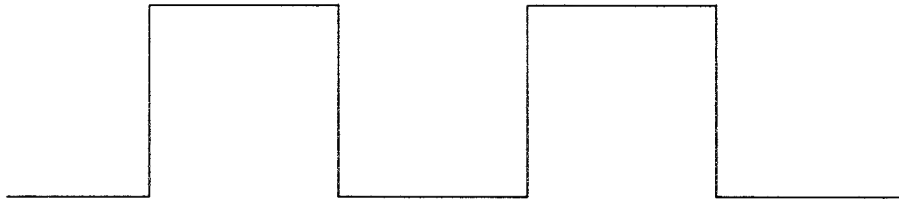
Fig. 8

DECLARATION FOR PATENT APPLICATION

Attorney Docket No: **061607-1100**

As the below named inventor, I hereby declare that:

Our residences, post office addresses and citizenships are as stated below next to our names.

We believe we are the original, first, and joint inventors of the subject matter which is claimed and for which a patent is sought on the invention entitled **CIRCUIT AND METHOD FOR DETECTING AND CORRECTING DATA CLOCKING ERRORS**, the specification of which:

☒ is attached hereto.
☐ was filed on ___ as Application Serial No. ___.
☐ was filed on ___ under U.S. Express Mail No. ___.
☐ is set forth in PCT International Application No. ___;
filed on ___ and as amended Under PCT Article 19 on ___ (if any).

I/we hereby state that I/we have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above.

I/we acknowledge the duty to disclose information which is material to the examination of this application in accordance with Title 37, Code of Federal Regulations, §1.56.

I/we hereby claim the benefit under Title 35, United States Code, §119 of any United States provisional patent application, foreign application(s) for patent or inventor's certificate listed below and have also identified below any United States provisional patent application, foreign application for patent or inventor's certificate having a filing date before that of the above-identified application on which priority is claimed: **U.S. Provisional Application Serial No. 60/101,467 entitled "Circuit for Automatically Inverting Data Clock Signal Upon Detection of Data Clocking Error" filed September 23, 1998**

I/we hereby claim the benefit under Title 35, United States Code, §120 of any United States patent application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, §112, I/we acknowledge the duty to disclose material information as defined in Title 37, Code of Federal Regulations, §1.56 which occurred between the filing date of the prior application and the national or PCT international filing date of this application: **NOT APPLICABLE.**

I/we hereby appoint the following attorneys/agents to prosecute this application and to transact all business in the Patent and Trademark Office connected therewith: **George M. Thomas, Reg. No. 22,260; James W. Kayden, Reg. No. 31,532; Scott A. Horstemeyer, Reg. No. 34,183; Stephen R. Risley, Reg. No. 35,659; Jeffrey R. Kuester, Reg. No. 34,367; Daniel J. Santos, Reg. No. 40,158; Daniel R. McClure, Reg. No. 38,962; Robert E. Stachler II, Reg. No. 36,934; David P. Kelley, Reg. No. 17,420; Michael J. Tempel, Reg. No. 41,344; Michael J. D'Aurelio, Reg. No. 40,977; David R. Risley, Reg. No. 39,345; Jon E. Holland, Reg. No. 41,077; Dan R. Gresham, Reg. No 41,805; M. Paul Qualey, Reg. No 43,024.**

Please address all telephone calls, in the first instance, to **Dan R. Gresham** at telephone number: **(770) 933-9500.**

Address all correspondence to:

Scott A. Horstemeyer
THOMAS, KAYDEN, HORSTEMEYER
& RISLEY, L.L.P.
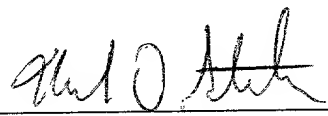**100 Galleria Parkway, N.W., Suite 1500**
Atlanta, Georgia 30339-5948

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statement and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Inventor's Signature: _____ Date: 7/12/99

Full Name of First or Sole Inventor: **Louis F. Villarosa, Jr.**
Residence: **2718 Palmetto Street, Tampa, Florida** Citizenship: **US**
Post Office Address: **2718 Palmetto Street**
Tampa, Florida

Inventor's Signature: _____ Date: 7/13/99

Full Name of Second Inventor: **Mark D. Studebaker**
Residence: **3042 Kevlyn Court, Safety Harbor, Florida** Citizenship: **US**
Post Office Address: **3042 Kevlyn Court**
Safety Harbor, Florida

Inventor's Signature: _____ Date: _____

Full Name of Third Inventor: _____
Residence: _____ Citizenship: _____
Post Office Address: _____
_____

DeclarPOA-Short.doc